IN THE CLAIMS

Please cancel claims 1-12 and add the following new claims.

13. (New) Method of storing data words in a RAM module, comprising the steps of:

producing a check bit word from at least one data word when writing the at least one data word into the RAM module,

storing the check bit word,

reading out the check bit word when reading out the at least one data word from the RAM module,

regenerating the check bit word from the at least one read-out data word,

comparing the read-out check bit word with the regenerated check bit word and generating an error message if they do not correspond.

14. (New) Method as claimed in claim 13, wherein the check bit word is generated by determining parity bits.

15. (New) Method as claimed in claim 14, wherein a 2 bit parity word is generated from each data word, and one parity bit is respectively determined from each half of the data word.

16. (New) Method as claimed in claim 13, wherein the check bit word is generated from a plurality of data words, and parity bits of the check bit word are respectively determined from equal digits of all data words.

17. (New) Method as claimed in claim 13, wherein the check bit words are generated by calculating CRC words.

18. (New) Method as claimed in claim 17, wherein a memory word is formed by summing a plurality of data words, and wherein an associated CRC word is calculated therefrom.

19. (New) Circuit configuration for storing data words in a RAM module, comprising:

a first circuit unit for generating a check bit word from at least one data word when writing and reading the at least one data word,

a plurality of registers for the allocated storage of check bit words for the data words, and

a second circuit unit by means of which, when reading data words, the associated check bit word is compared to the check bit word regenerated by the first circuit unit, and for generating an error message if the check bit words do not correspond.

20. (New) Circuit configuration as claimed in claim 19, wherein the number of registers in said plurality of registers is determined by including one 2-bit parity register for each data word.

21. (New) Circuit configuration as claimed in claim 19, wherein the number of registers in said plurality of registers is determined by including one CRC register for each four data words.

22. (New) Circuit configuration as claimed in claim 21, further including a multiplexer for storing four data words as one memory word, and a CRC arithmetic unit for calculating the CRC word from a memory word and for storing the CRC word in an associated CRC register.

23. (New) Circuit configuration as claimed in claim 22, wherein the data words are 32 bits long and the CRC words are 9 bits long.

24. (New) Circuit configuration as claimed in claim 19, further including a global check bit word register for storing a global check bit word, the bits of which are respectively determined from equal digits of all data words, and an associated register for storing a check bit word which is determined from the contents of the global register.